Bias-Stress Instability in GaN Field-Effect Transistors

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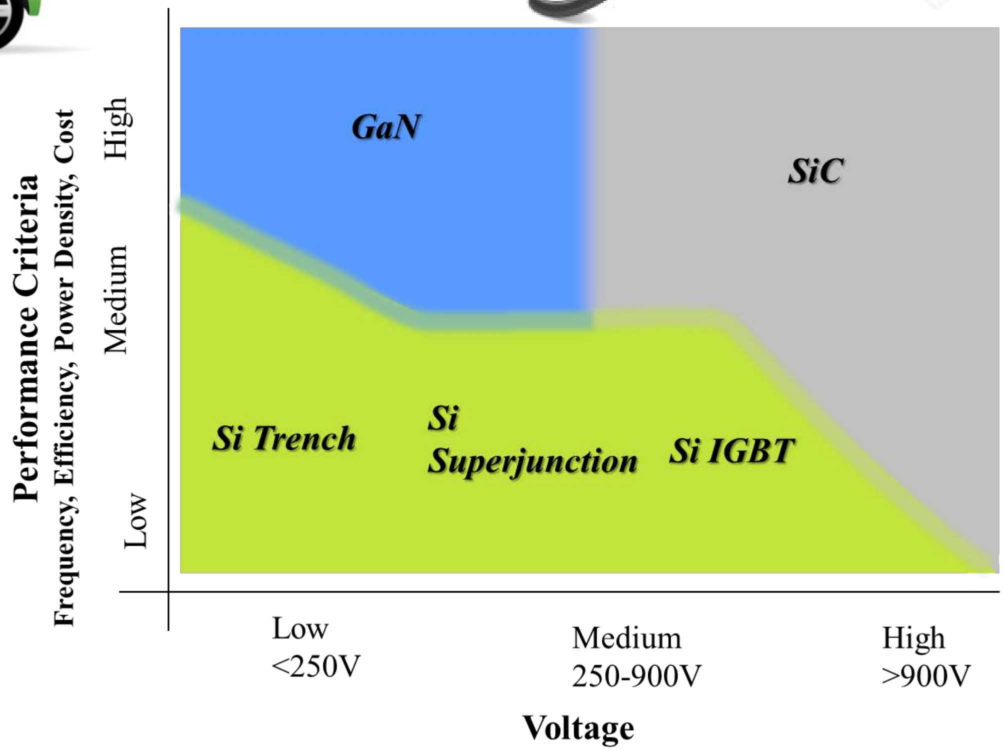
Acknowledgements:

- S. Warnock (MIT Lincoln Lab.), J. Franco (IMEC)
- Sponsors: MIT-MTL GaN Energy Initiative, NDSEG Fellowship

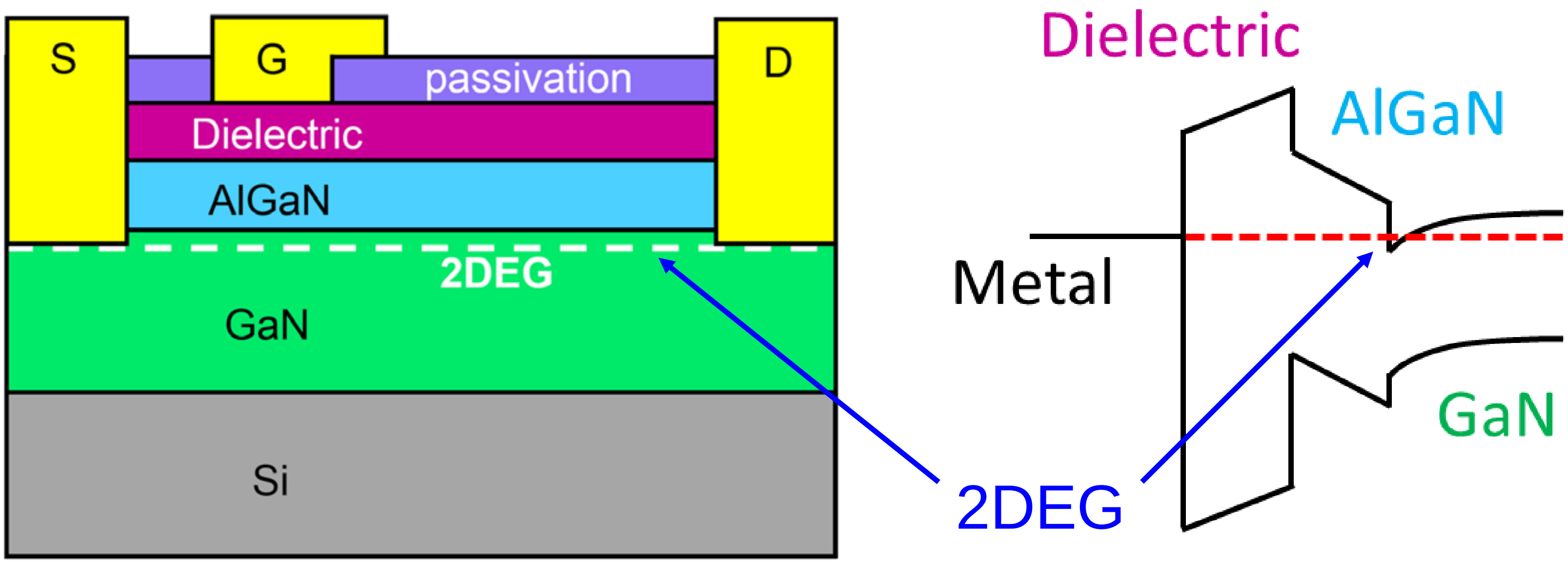
Application space
for future power electronics



Important role for GaN power electronics in future

Favored structure: GaN MIS-HEMT

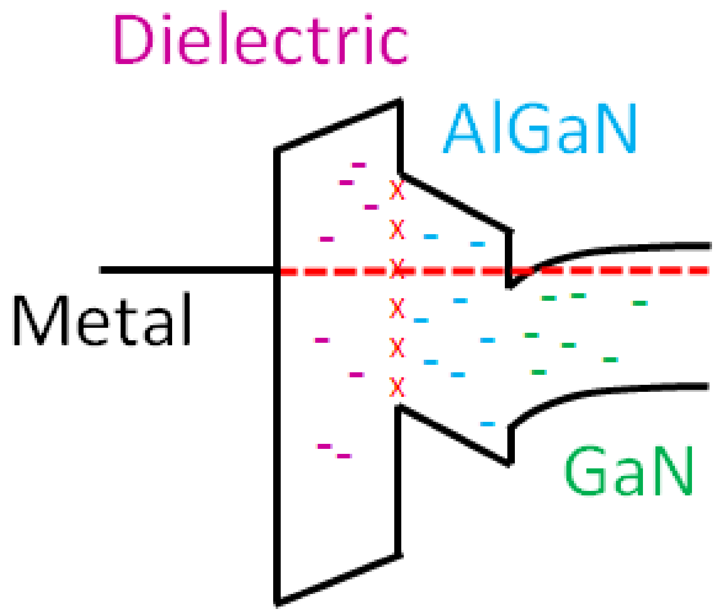
- MIS-HEMT: Metal-Insulator-Semiconductor High Electron Mobility Transistor



- High-mobility 2DEG at AlGaN/GaN interface
- Dielectric to suppress gate leakage current and increase gate swing
- On Si for low cost

Main concern with GaN MIS-HEMTs: reliability and stability

- Si substrate → defects in GaN
- Multiple interfaces, many trapping sites

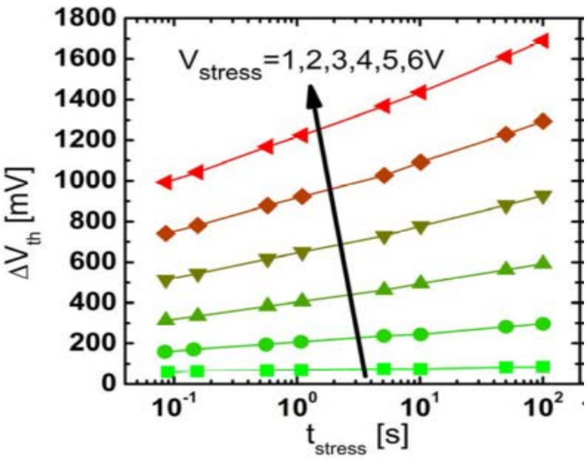


- Uncertain electric field distribution across gate stack

Bias-Temperature Instability (BTI)

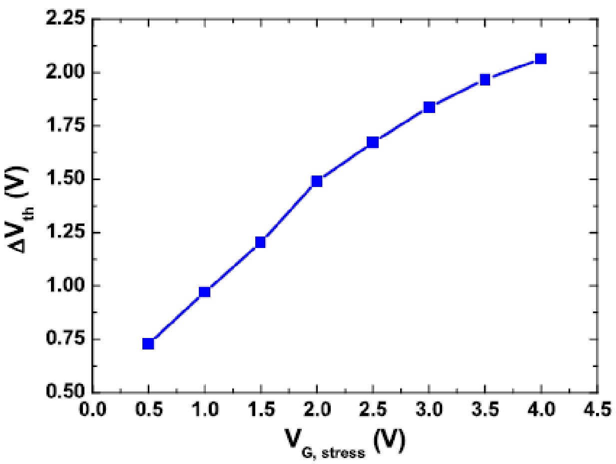
Device stability during operation: key concern, particularly V_T

Al_2O_3/AlGaN/GaN



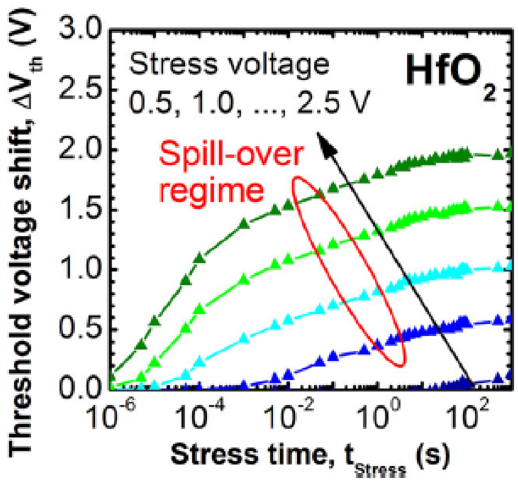
Lagger, IEDM 2012

SiN/AlGaN/GaN



Zhang, SST 2014

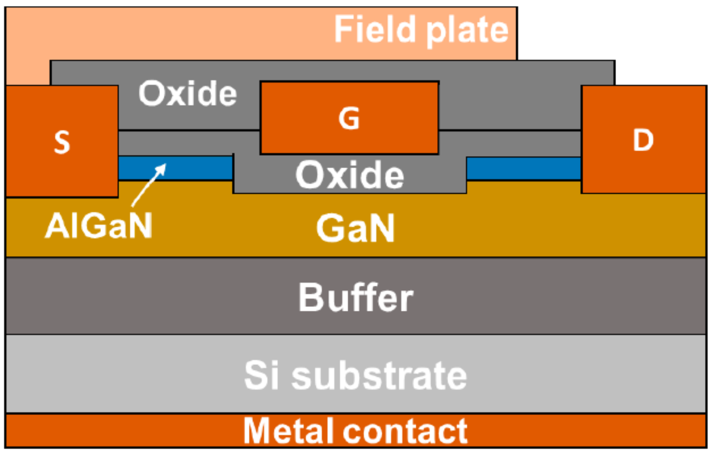
HfO_2/AlGaN/GaN

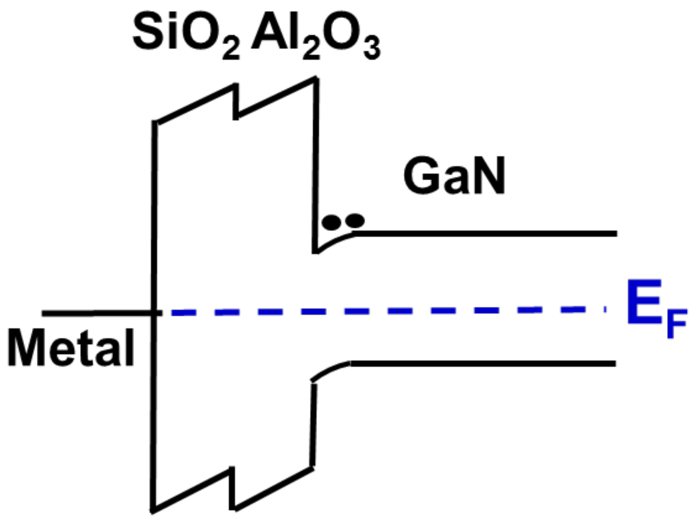


Winzer, PSSa 2016

BTI in GaN MOSFETs

Simpler than MIS-HEMTs: single GaN/oxide interface



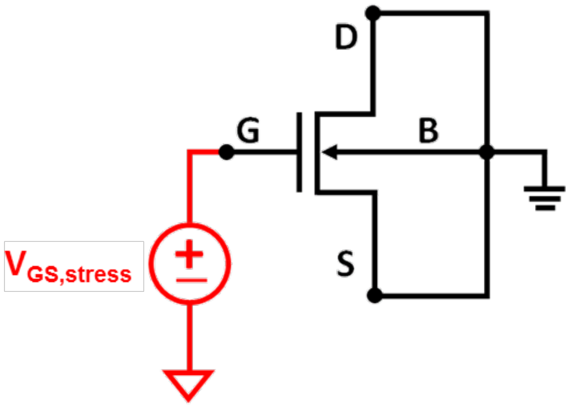


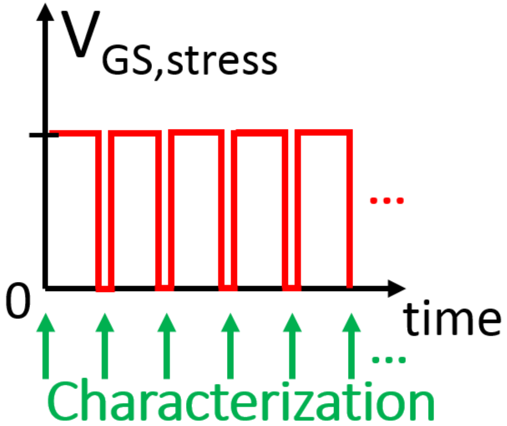
- Industrial prototype devices
- Gate dielectric: SiO_2/Al_2O_3 (EOT=40 nm)

Guo, IRPS 2015
Guo, IRPS 2016
Guo, TED 2017

Experimental methodology

Constant-V_{GS}, stress-interrupt experiments at RT:





Guo, TED 2017

1. Device initialization through thermal detrapping step

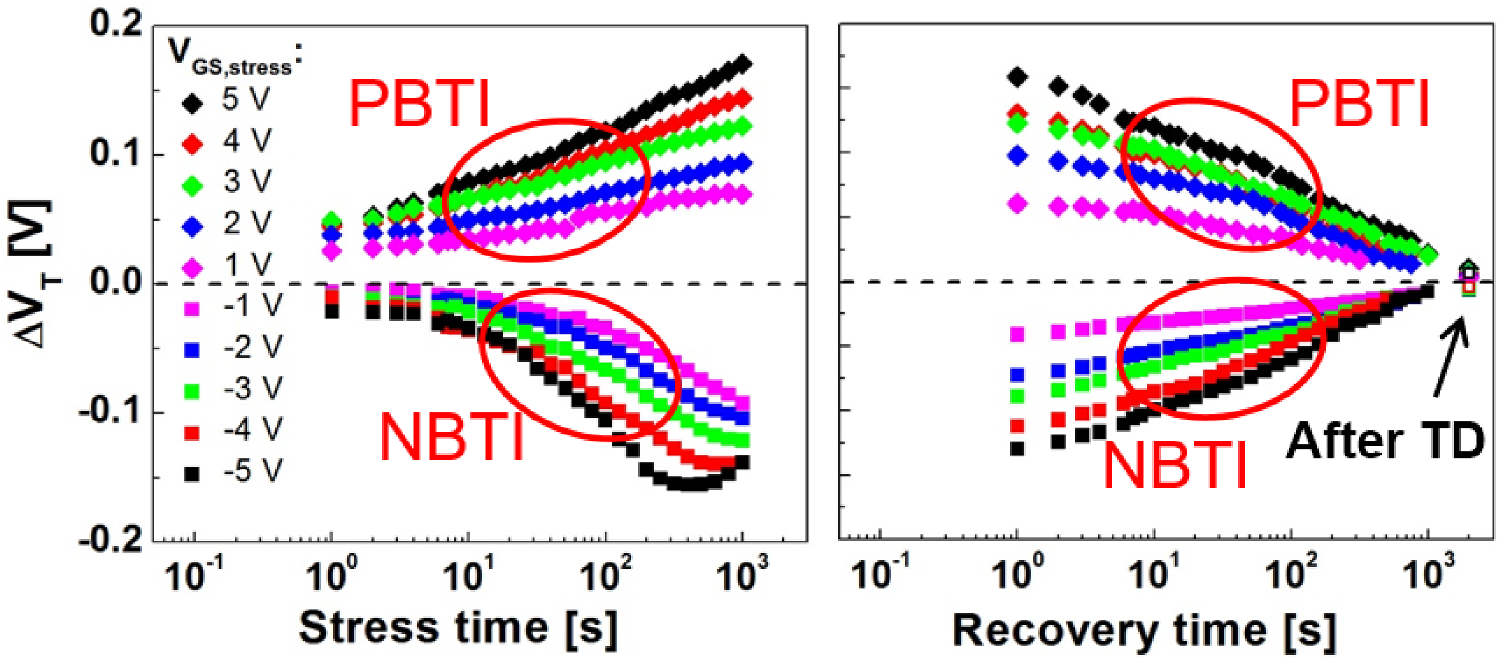
   Minor impact: $\Delta V_T < 20$ mV, $\Delta S < 30$ mV/dec

2. Stress and characterization: measure V_T, peak g_m, S at V_{DS}=0.1 V

   After 50 characterization runs: $\Delta V_T < 10$ mV, $\Delta g_m < 0.02$ mS/mm, $\Delta S < 15$ mV/dec

3. Recovery phase with terminals grounded and periodic characterization
4. Final thermal detrapping

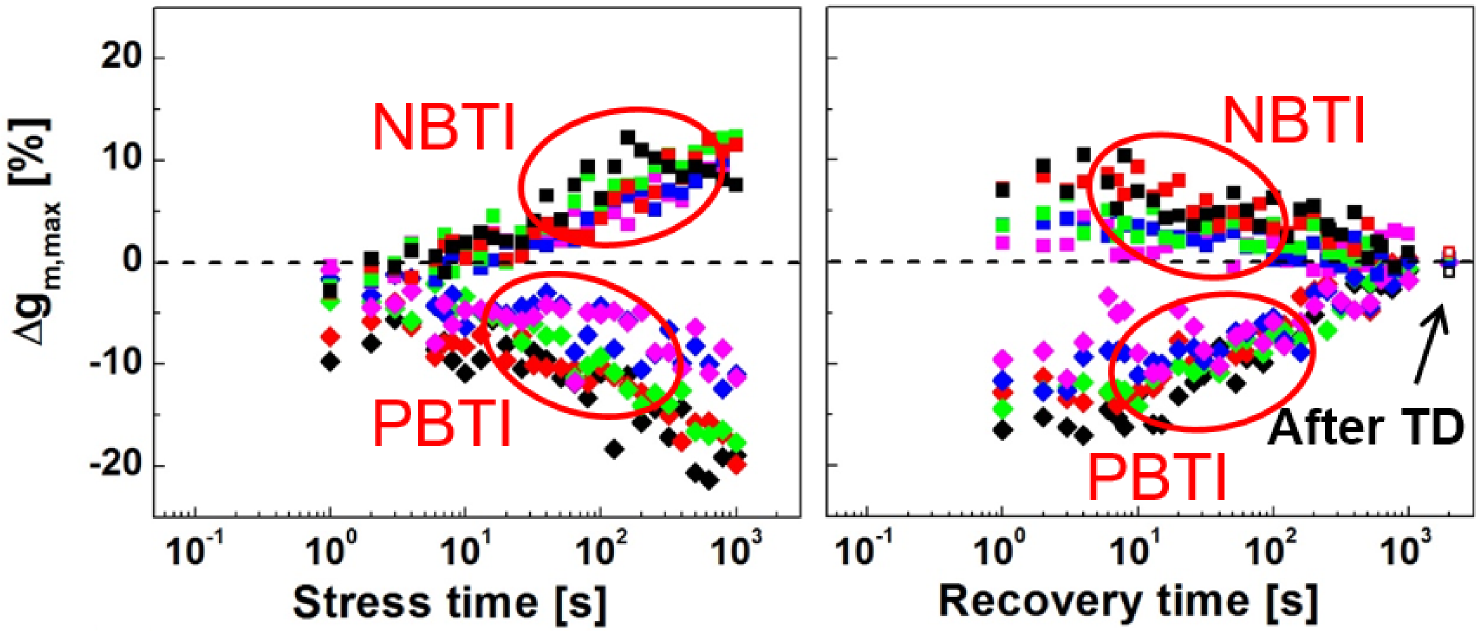
Threshold voltage evolution



- PBTI: $V_{GS,stress}>0 \rightarrow \Delta V_T>0$
- NBTI: $V_{GS,stress}<0 \rightarrow \Delta V_T<0$
- $|\Delta V_T|$ increases with stress voltage and time
- Fully recoverable → no defect generation

Guo, TED 2017

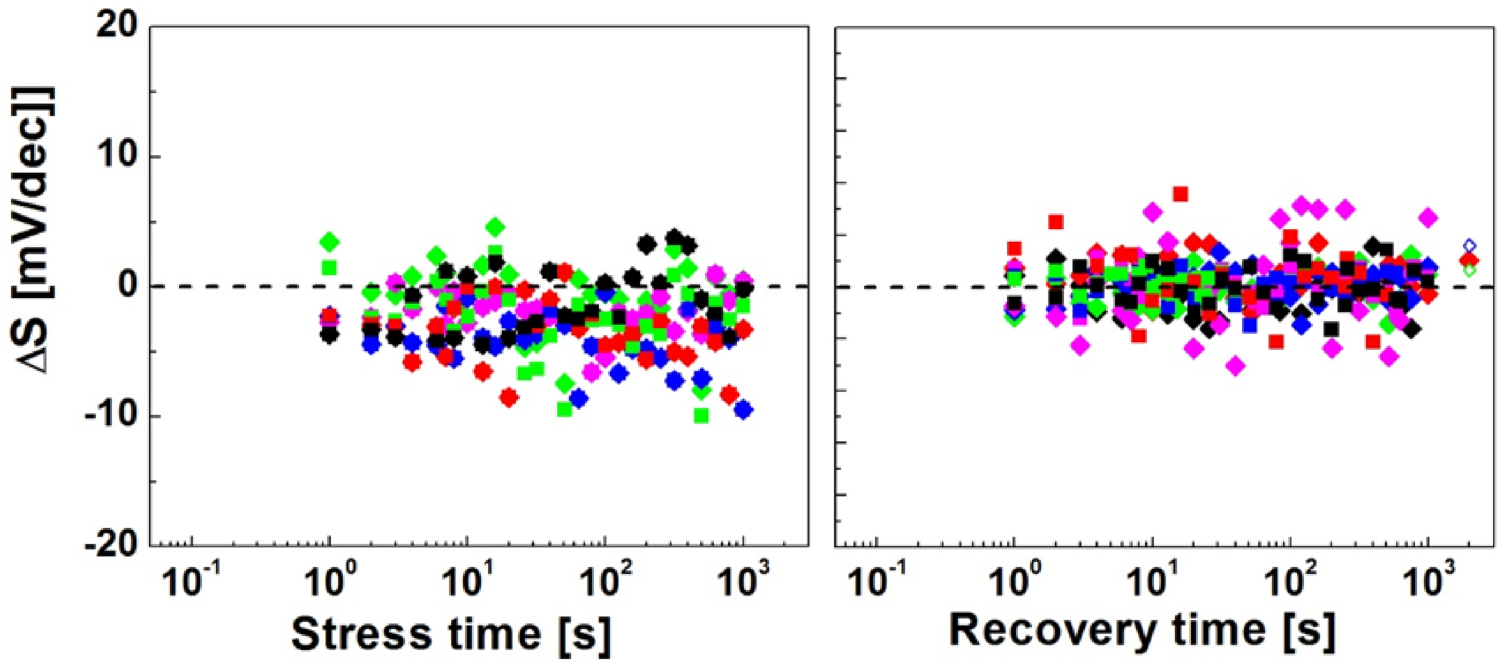
Transconductance evolution



Guo, TED 2017

- PBTI: $V_{GS,stress}>0$ → $g_{m,max}$↓
- NBTI: $V_{GS,stress}<0$ → $g_{m,max}$↑
- $|\Delta g_m|$ increases with stress voltage and time
- Fully recoverable → no defect generation

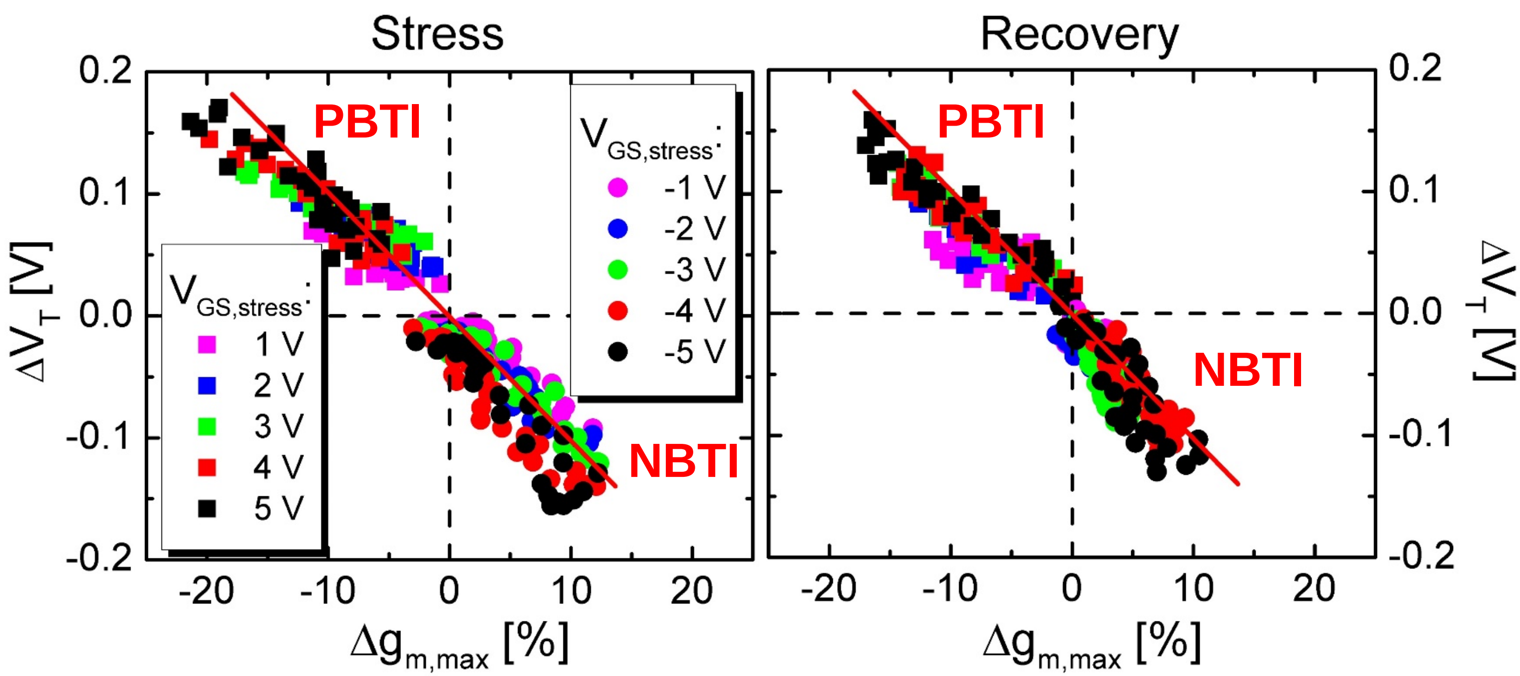
Subthreshold swing evolution



Guo, TED 2017

- PBTI: $V_{GS,stress}>0$ → S unchanged
- NBTI: $V_{GS,stress}<0$ → S unchanged
- No interface state generation

Correlation between ΔV_T and Δg_m

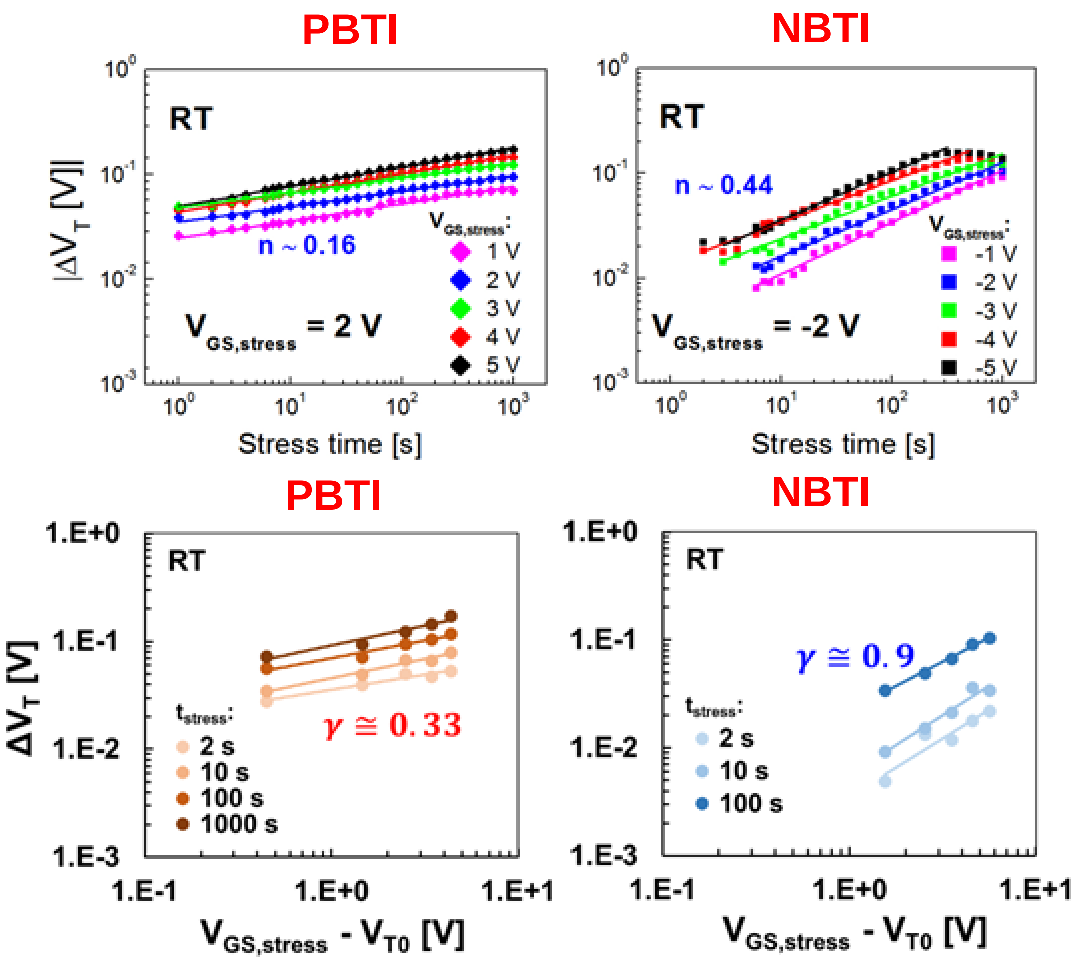


Guo, TED 2017

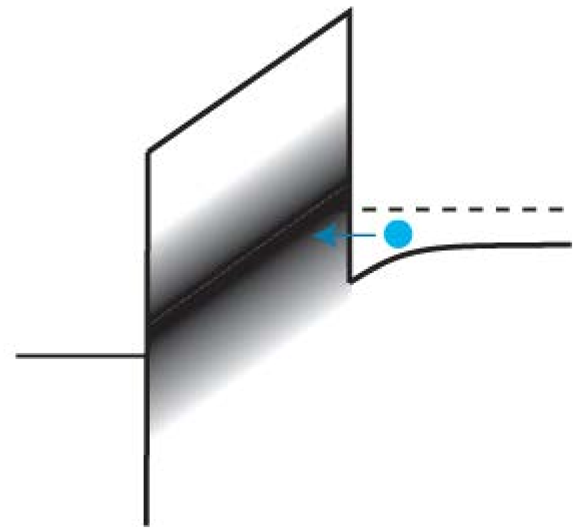
- Good correlation between PBTI and NBTI during stress and recovery
- One physical mechanism, fully reversible

Functional dependence of V_T

V_T well described by *power-law function*:



$$\Delta V_T \propto (V_{GS,stress} - V_{T0})^{\gamma}\, t^{n}_{stress}$$

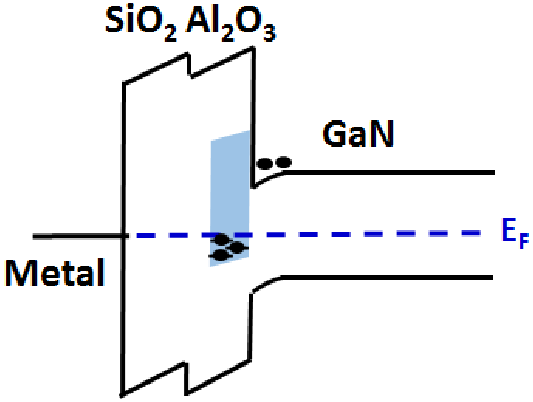


Guo, TED 2017

Consistent with electron trapping/detrapping in oxide

PBTI/NBTI: Recoverable electron trapping/detrapping in oxide

Initial



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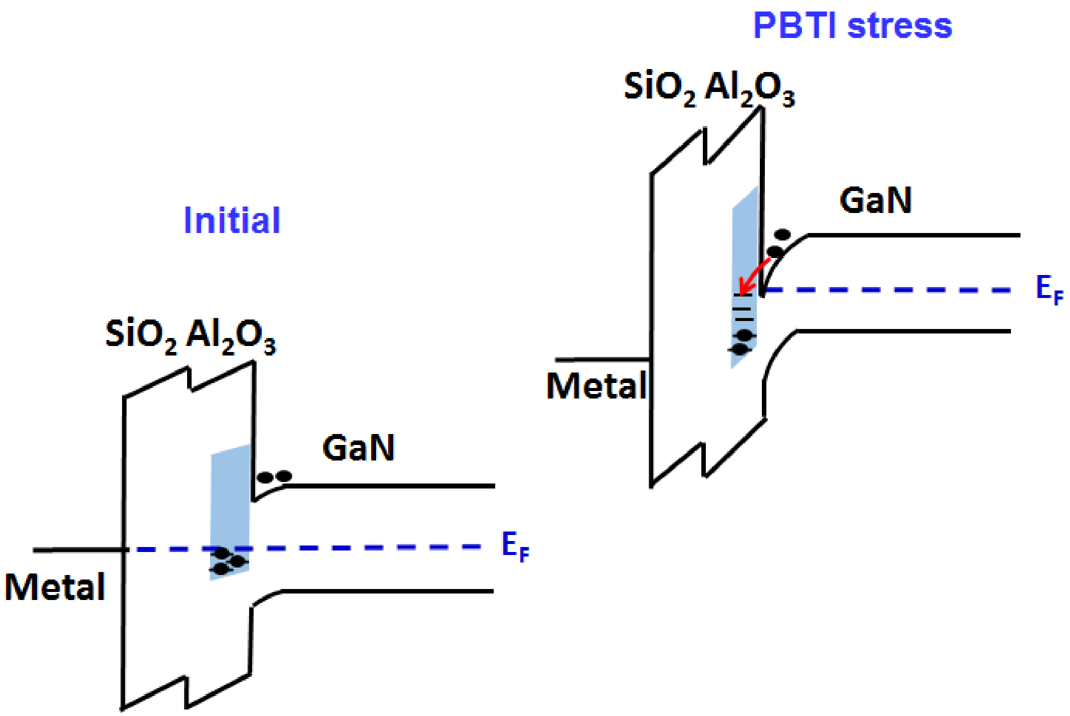

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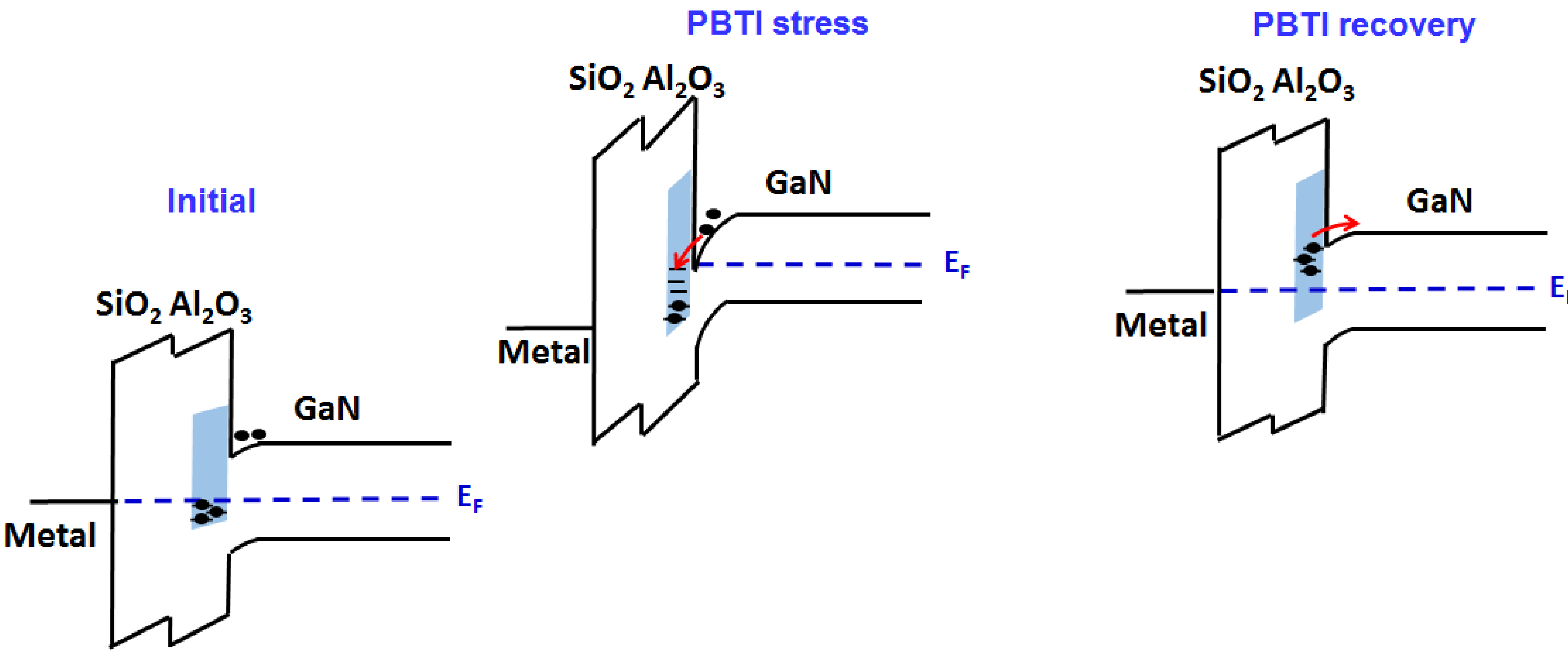

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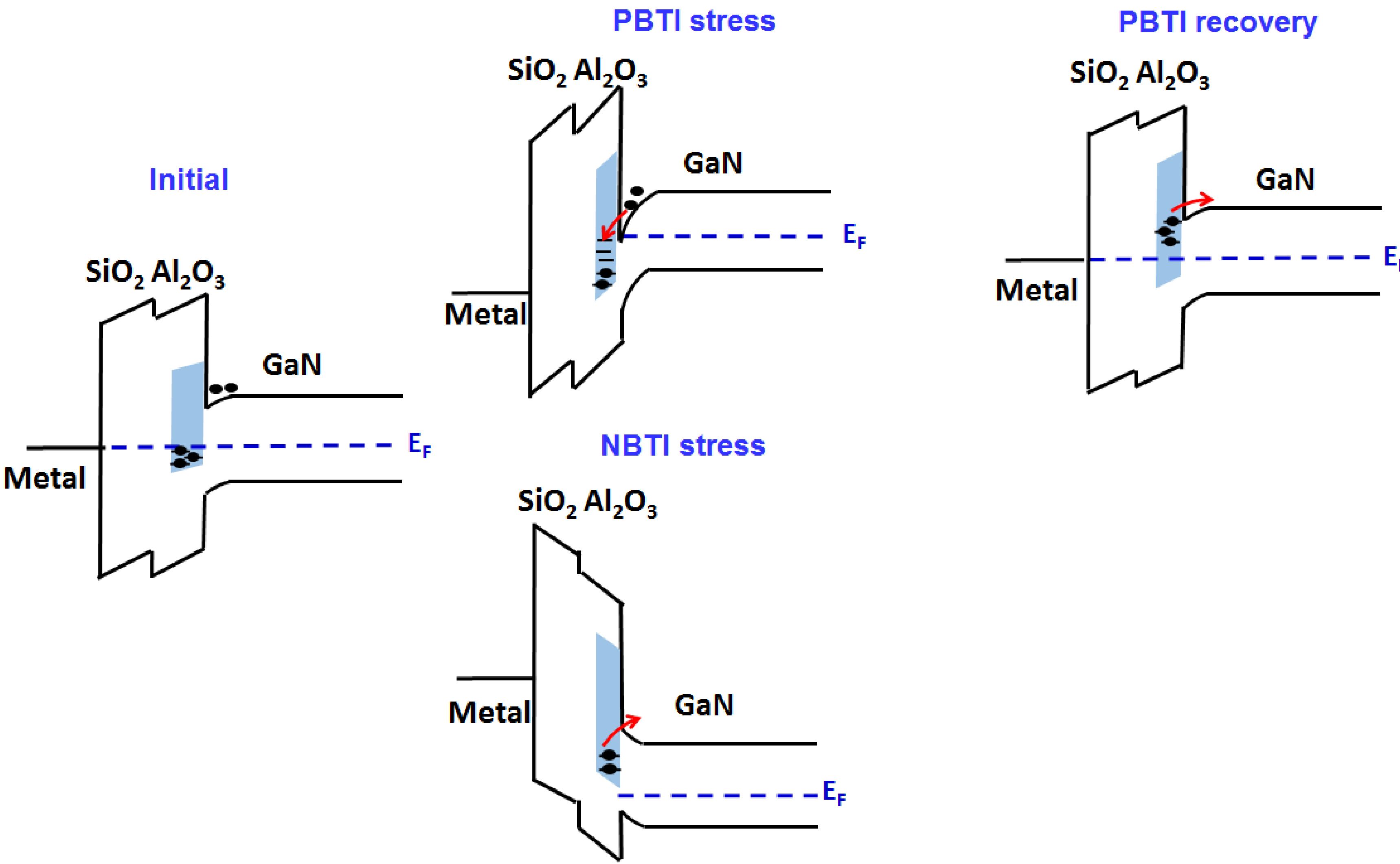

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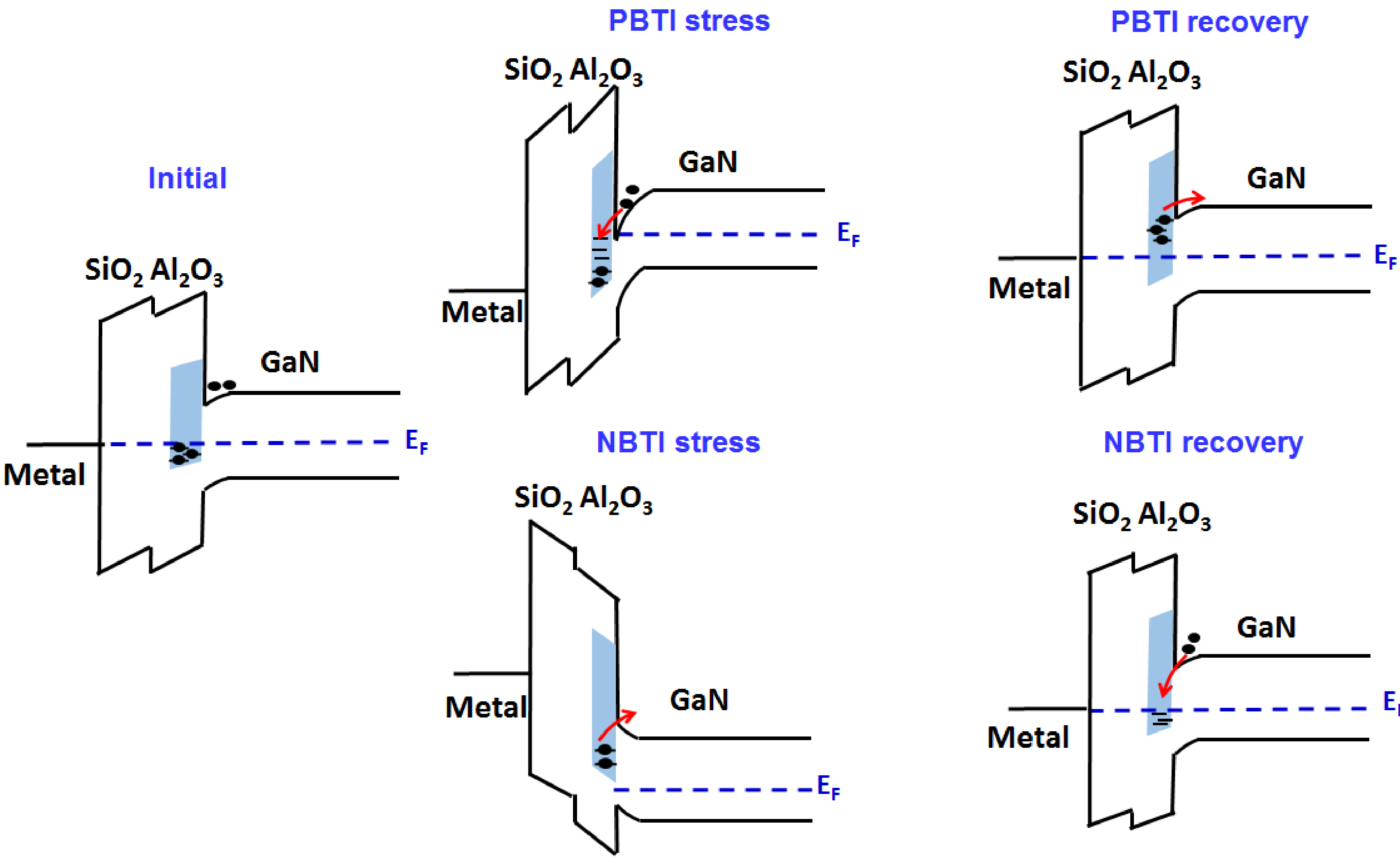
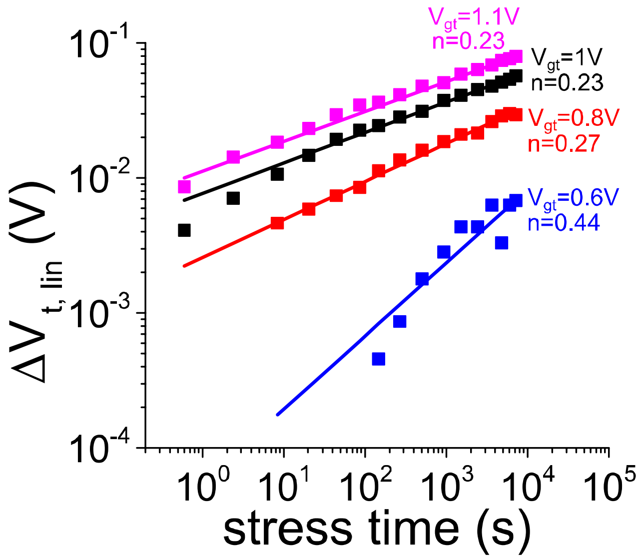
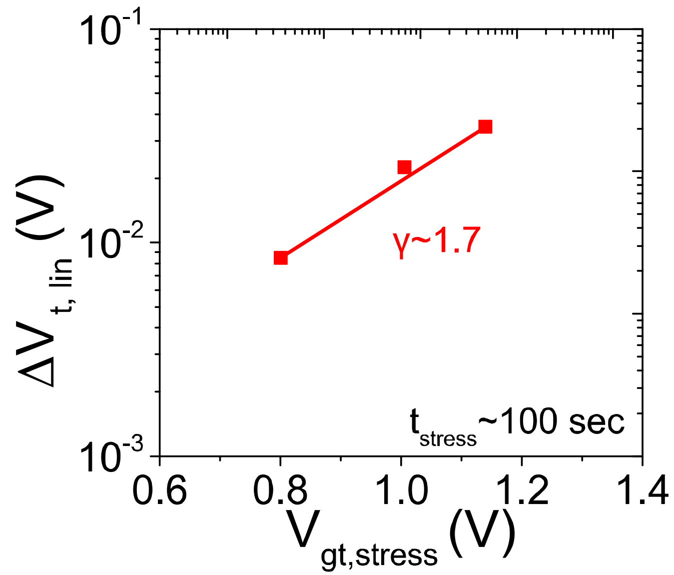
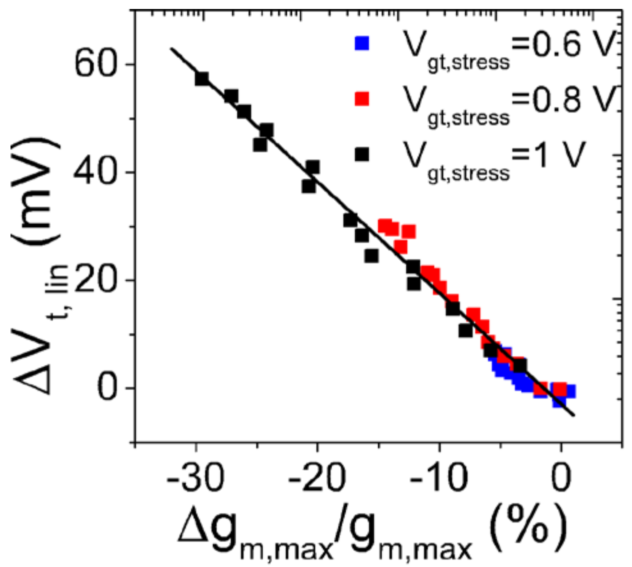
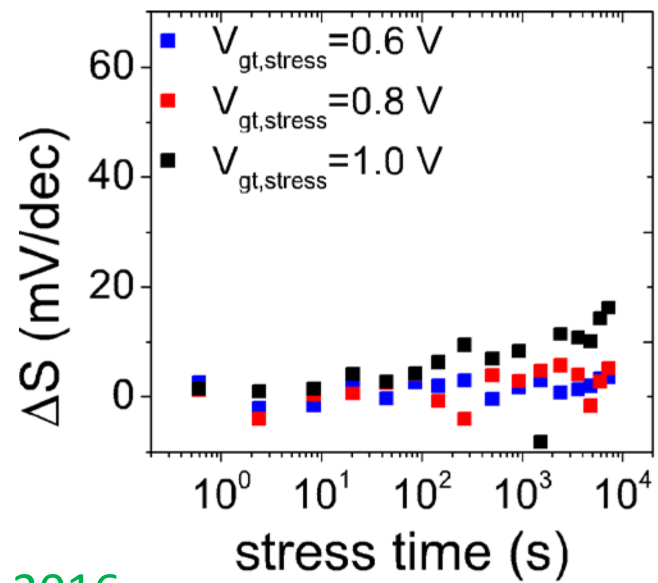


PBTI in HfO_2/InGaAs system





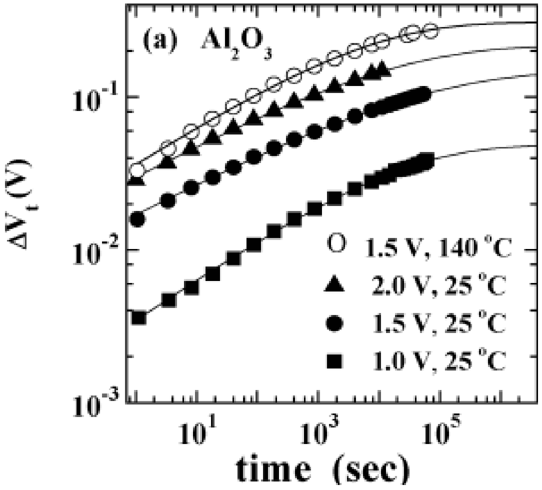




Cai, IEDM 2016

Oxide trapping in other high-k/MOS systems

Al_2O_3/Si



Zafar, TDMR 2005

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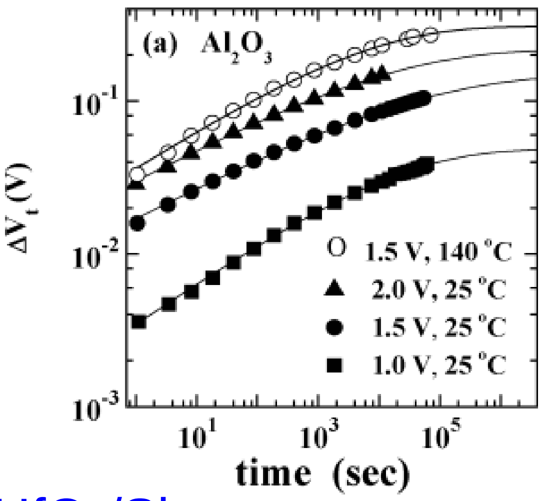

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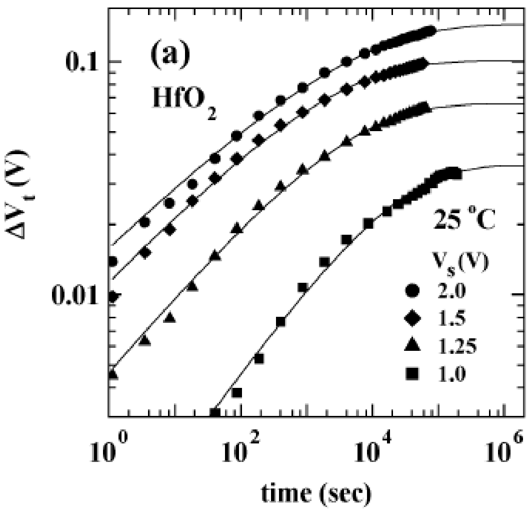

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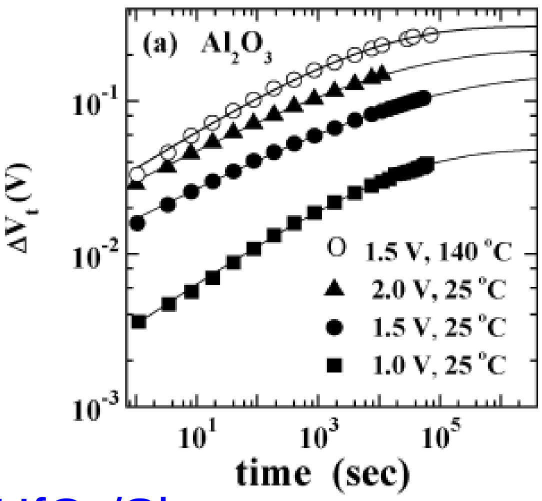
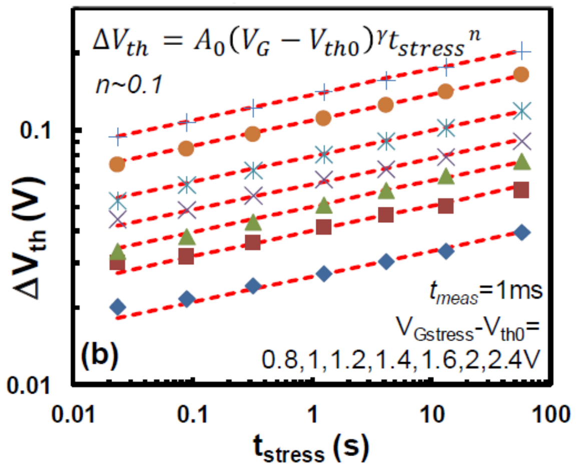


$Al_2O_3/InGaAs$



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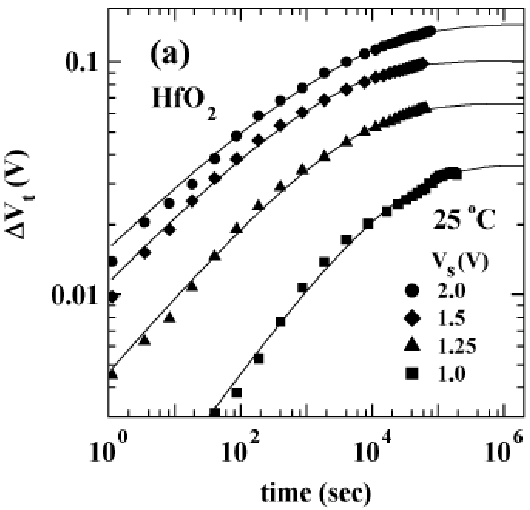

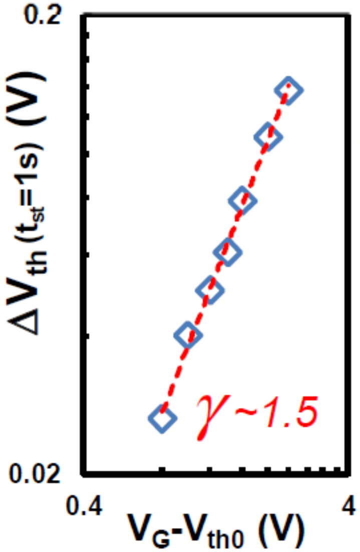

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Franco, IRPS 2014

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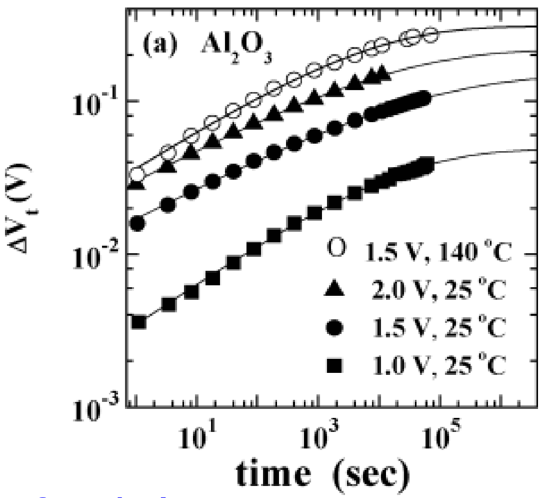

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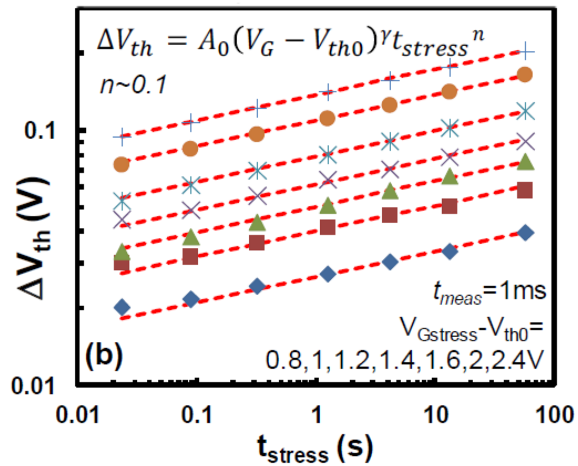
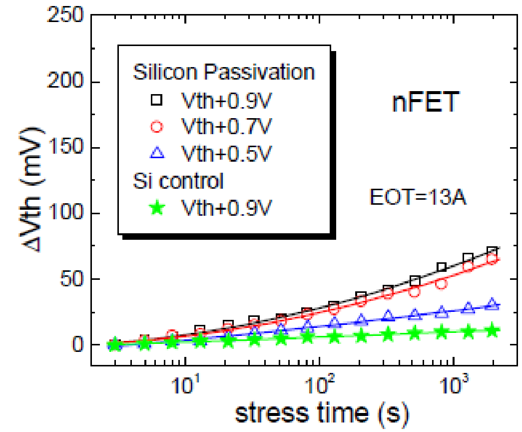


HfO_2/Ge



Wu, IEDM 2005

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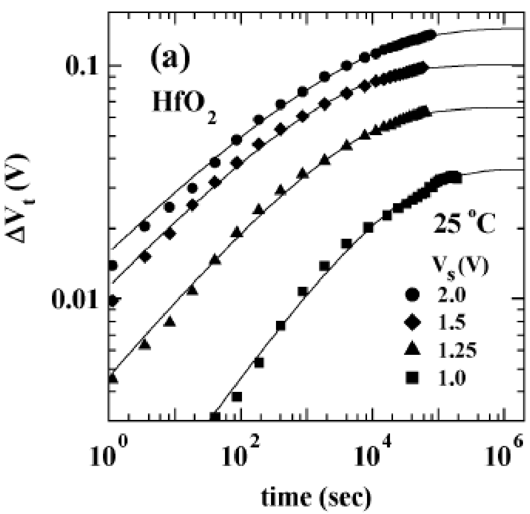
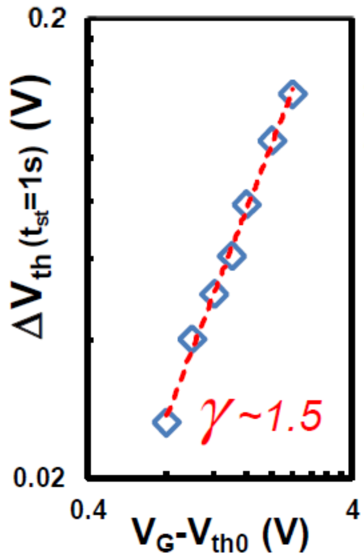


Zafar, TDMR 2005



Franco, IRPS 2014

Oxide trapping in other high-k/MOS systems

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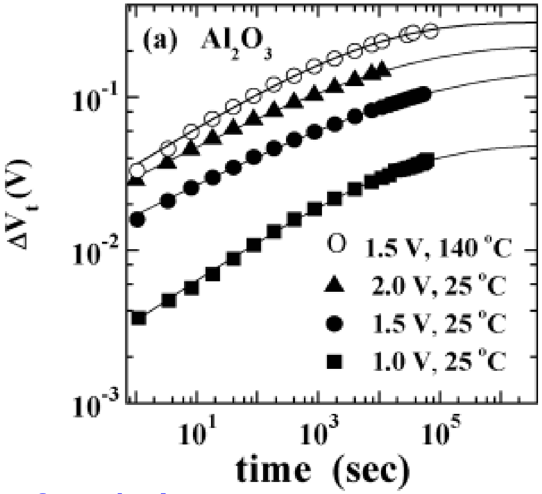

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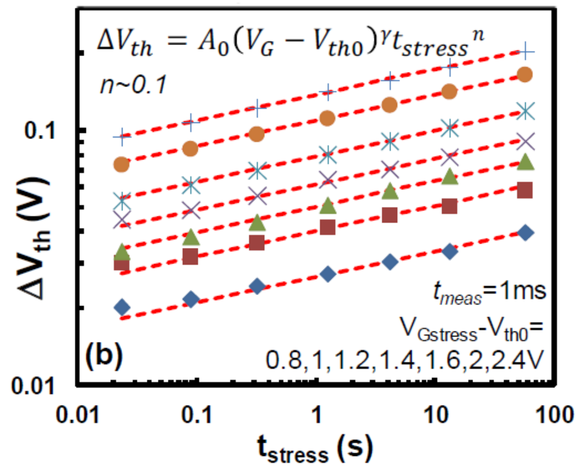

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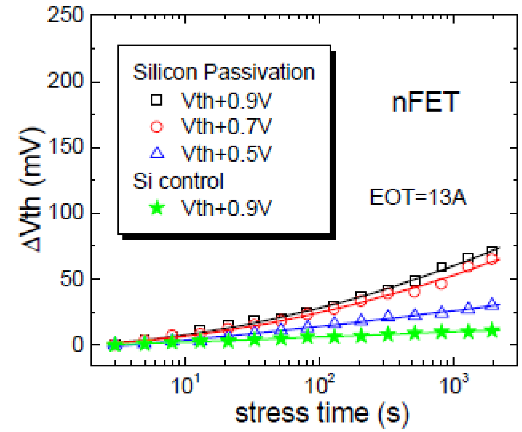

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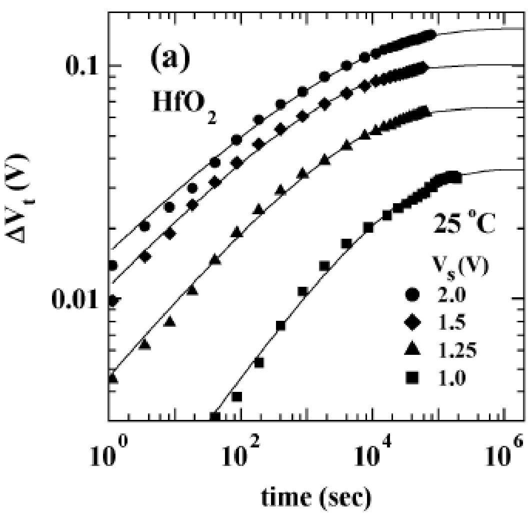

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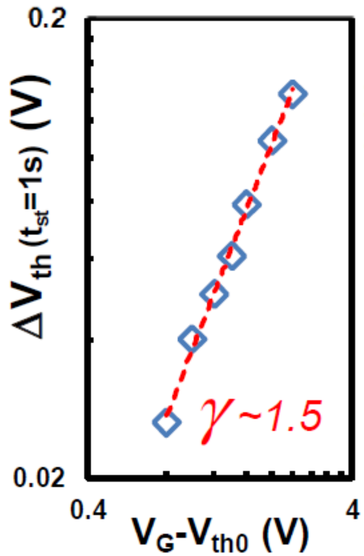
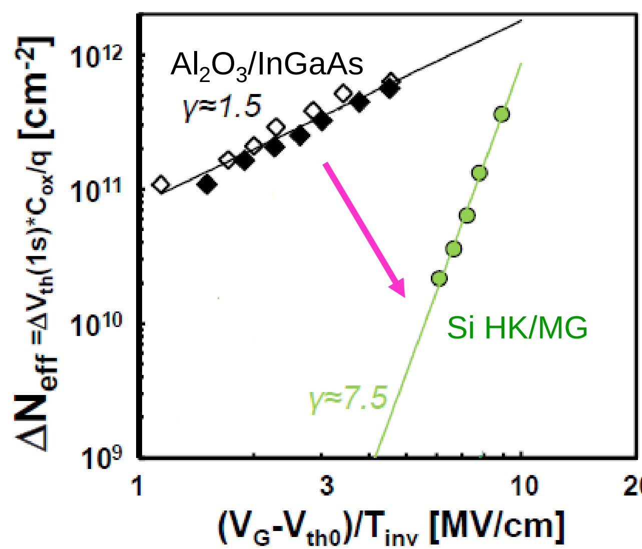


Franco, IRPS 2014

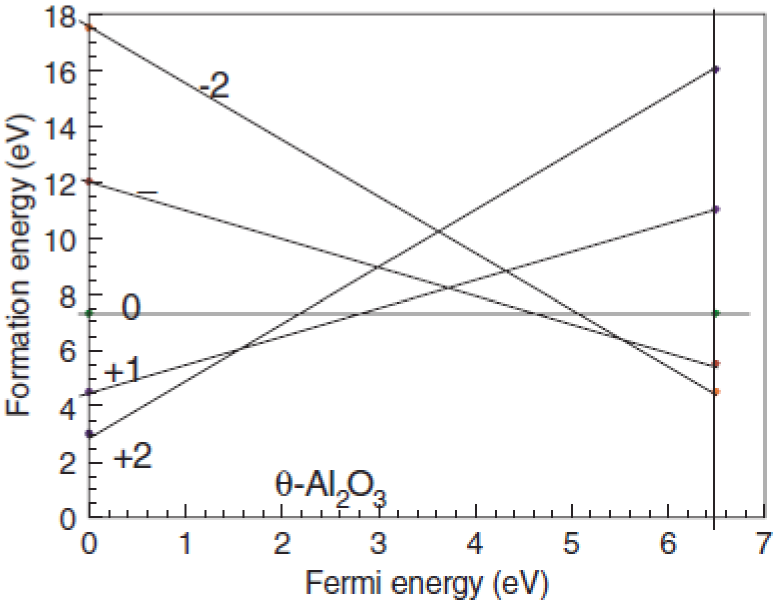


Franco, IEDM 2017

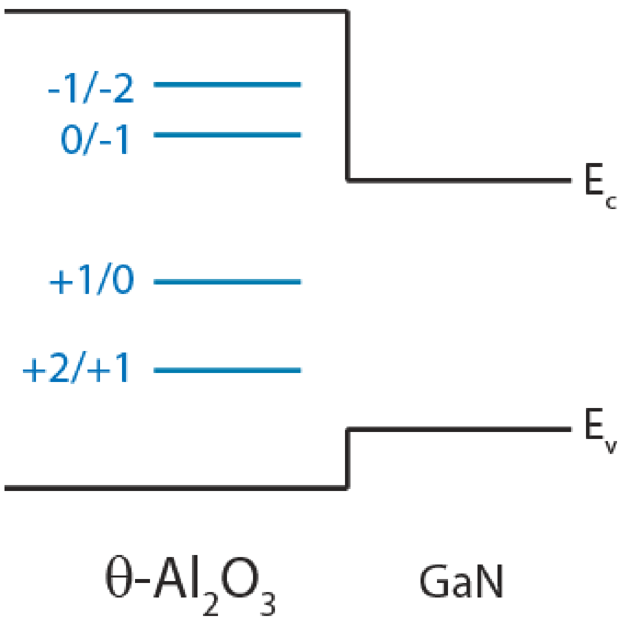
What are these defects?

Prime suspect: O vacancies

Formation energy of O vacancies:



Al_2O_3/GaN band alignment:



Liu, APL 2010

Defect states in Al_2O_3 right above conduction band edge of GaN

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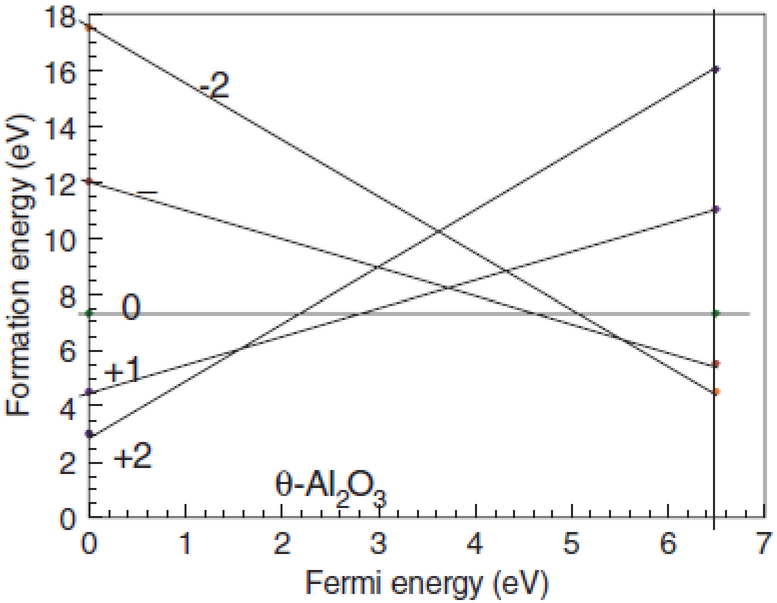

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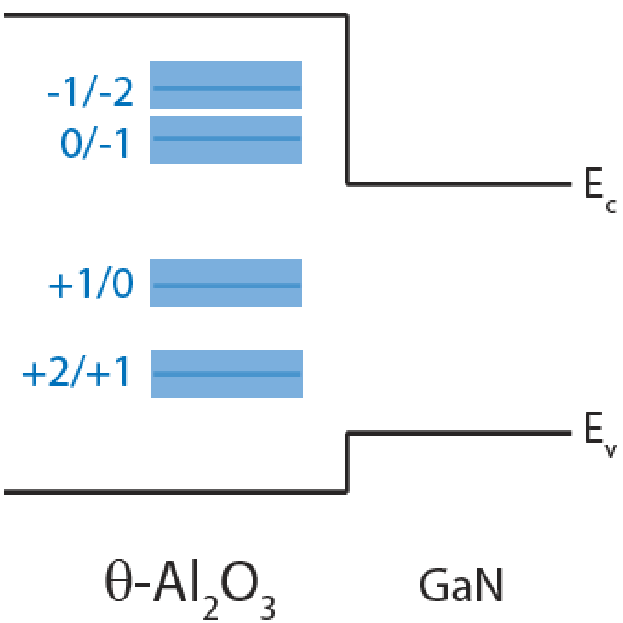

Liu, APL 2010

Defect states smear into bands in amorphous material

How to mitigate?

How to mitigate? Look at CMOS literature

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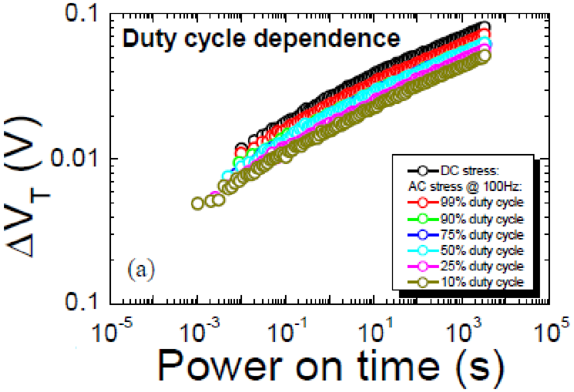
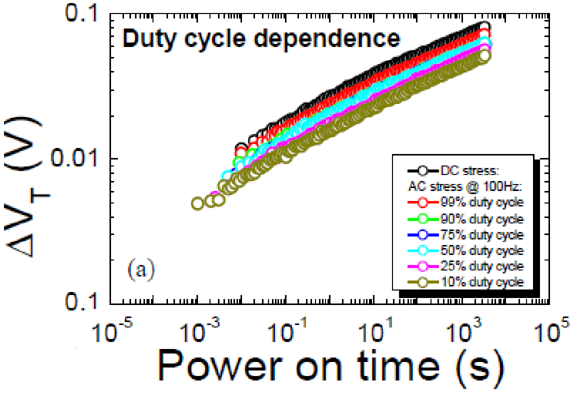


AC BTI more benign

Krishnan, IRPS 2012

How to mitigate? Look at CMOS literature



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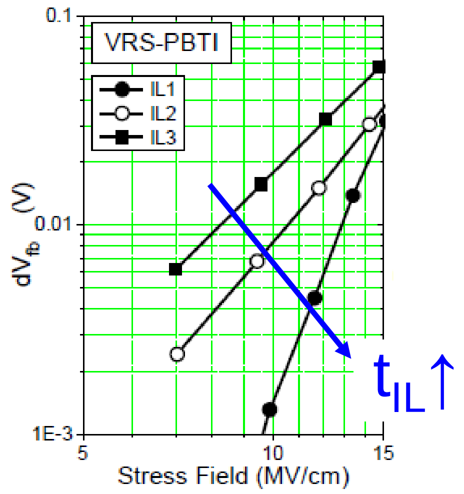
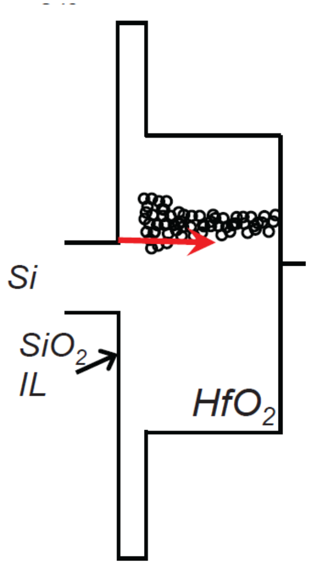


Introduce SiON interfacial layer Cartier, IEDM 2011



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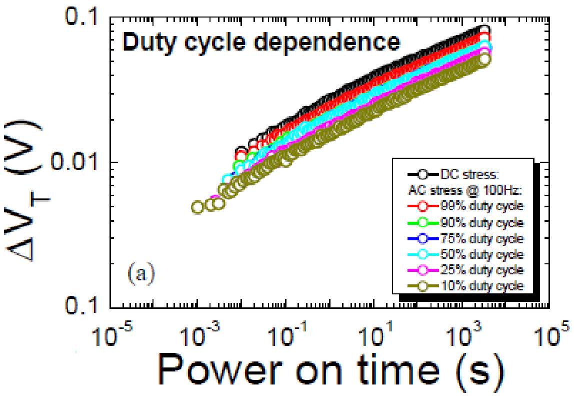

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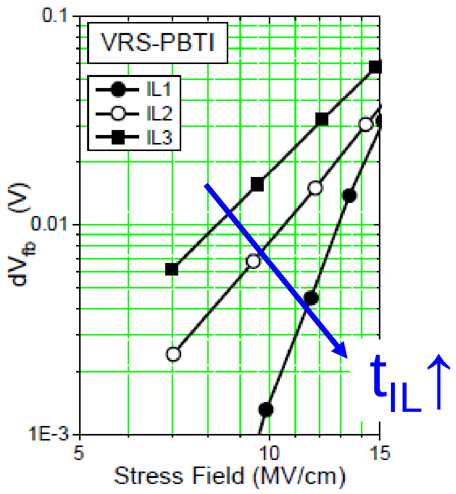

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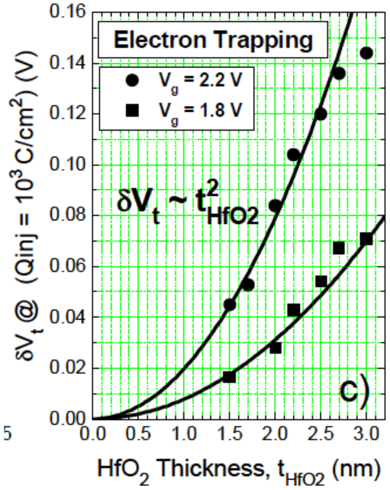
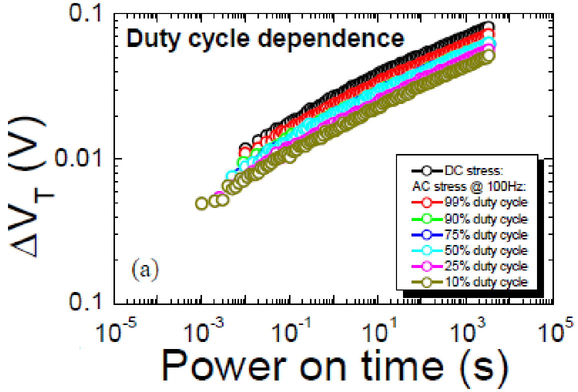


Reduce high-k thickness

Cartier, IEDM 2011

How to mitigate? Look at CMOS literature



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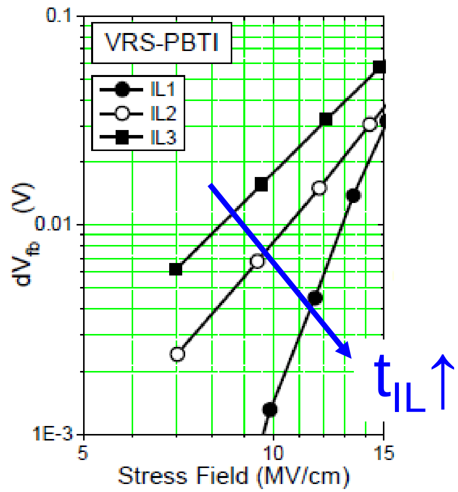

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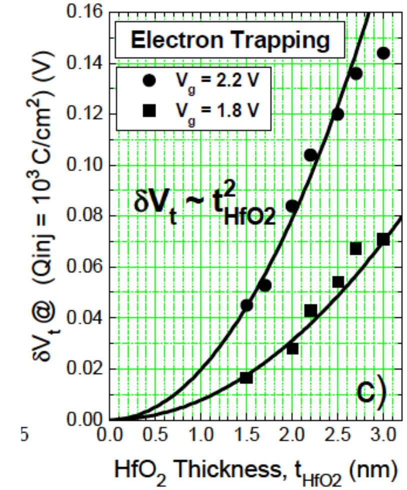

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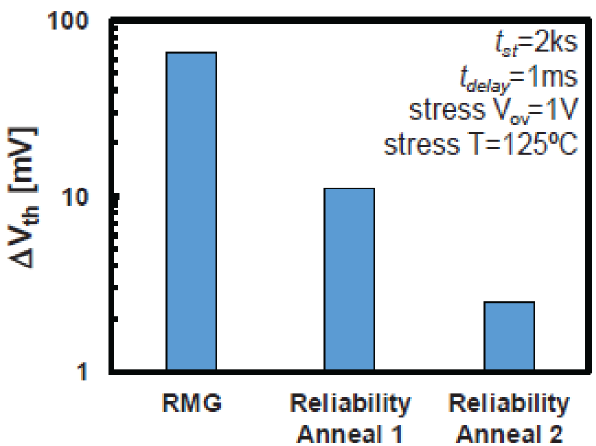

Short, high-T anneal

Franco, IRPS 2017

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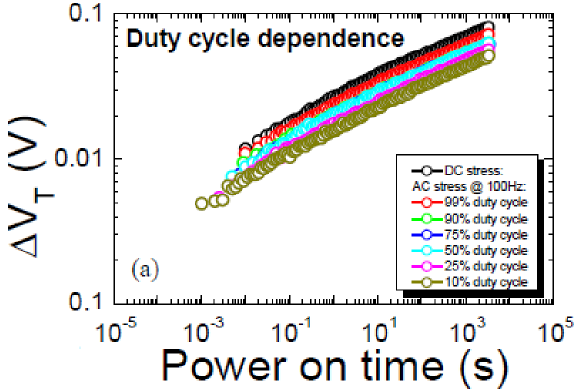

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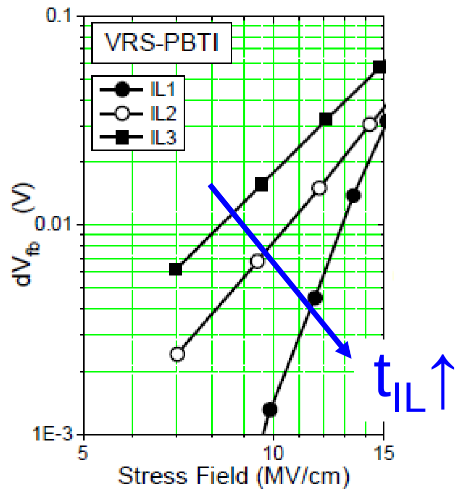

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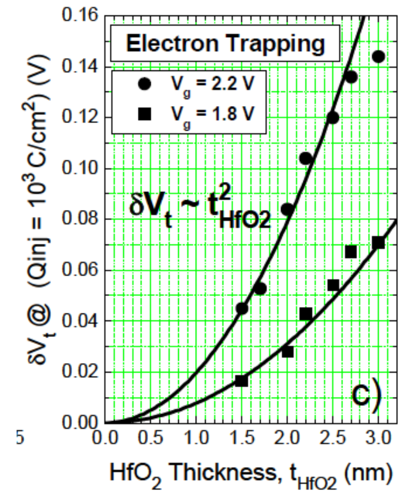
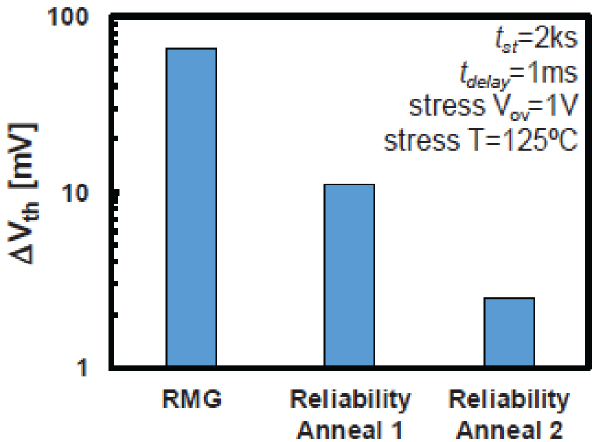


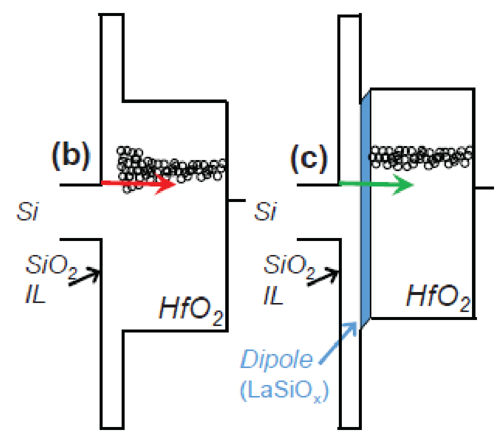
Reduce high-k thickness

Cartier, IEDM 2011



Short, high-T anneal

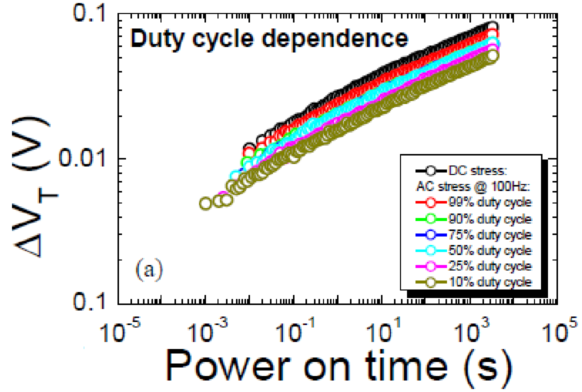
Franco, IRPS 2017



LaSiO interlayer

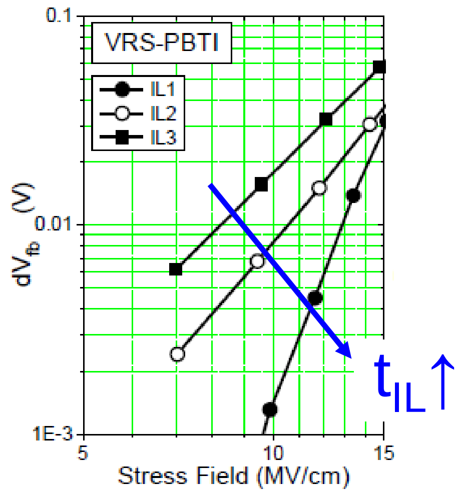
Franco, IRPS 2017

How to mitigate? Look at CMOS literature

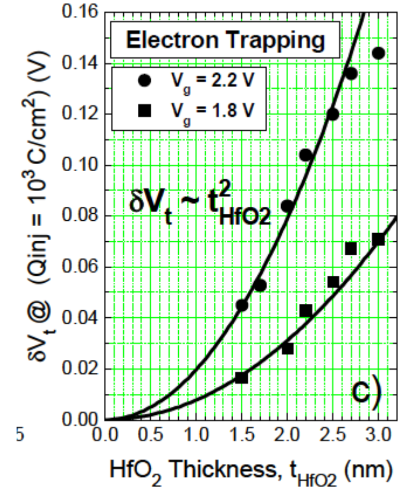


AC BTI more benign

Krishnan, IRPS 2012

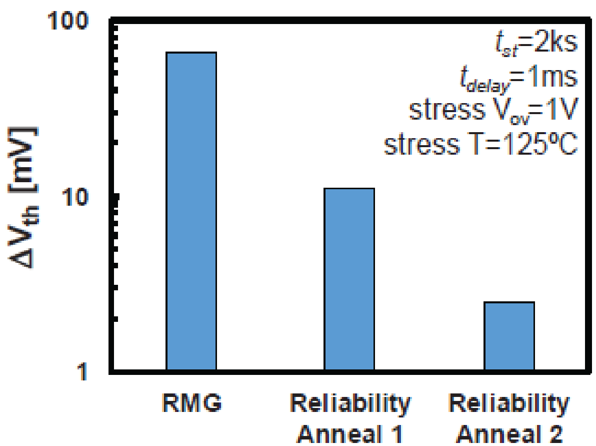


Introduce SiON interfacial layer Cartier, IEDM 2011



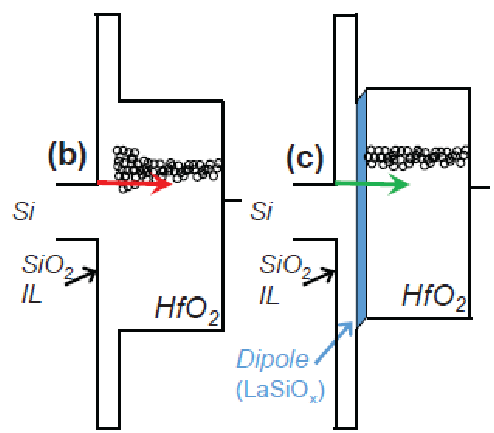
Reduce high-k thickness

Cartier, IEDM 2011



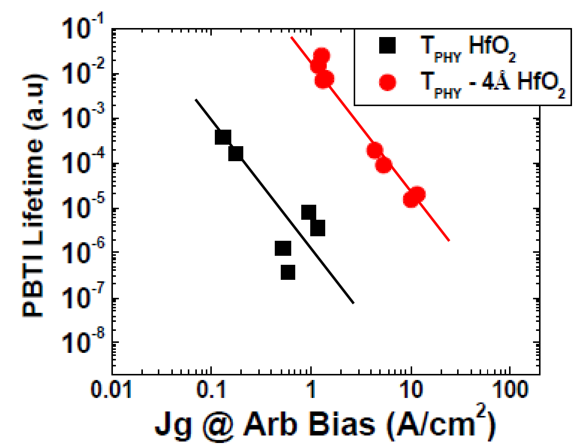
Short, high-T anneal

Franco, IRPS 2017



LaSiO interlayer

Franco, IRPS 2017

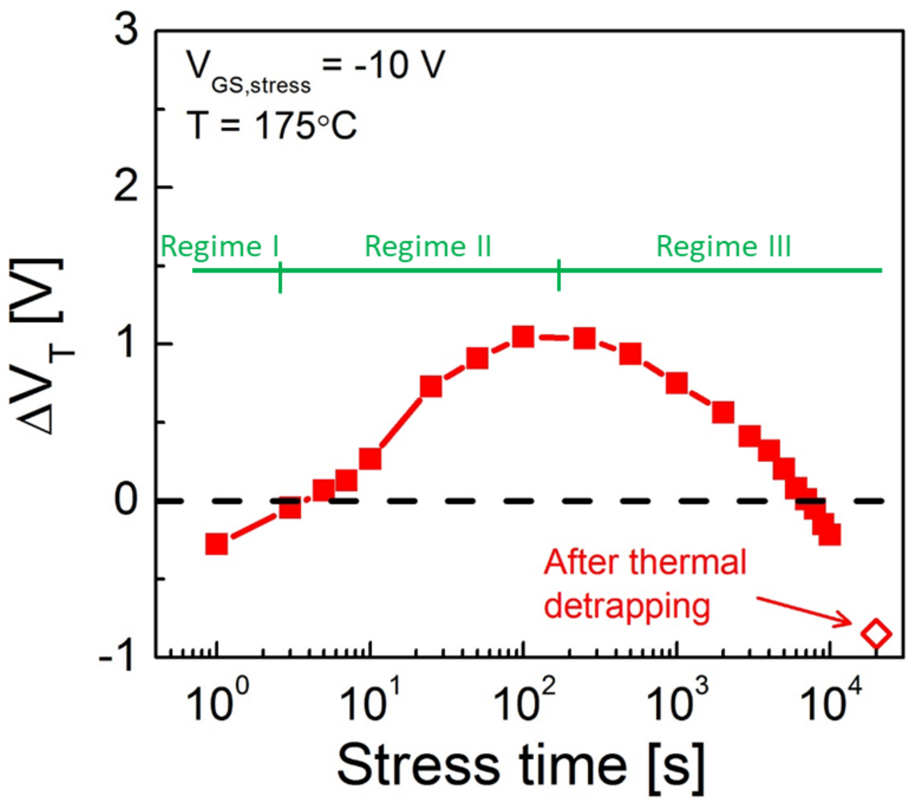


Reduce I_G

Krishnan, IRPS 2012

NBTI under harsher stress

High-voltage and high-temperature stress:



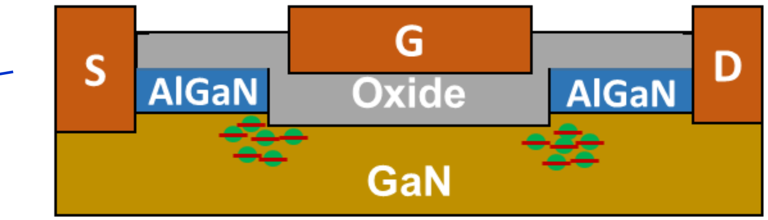
Guo, IRPS 2016

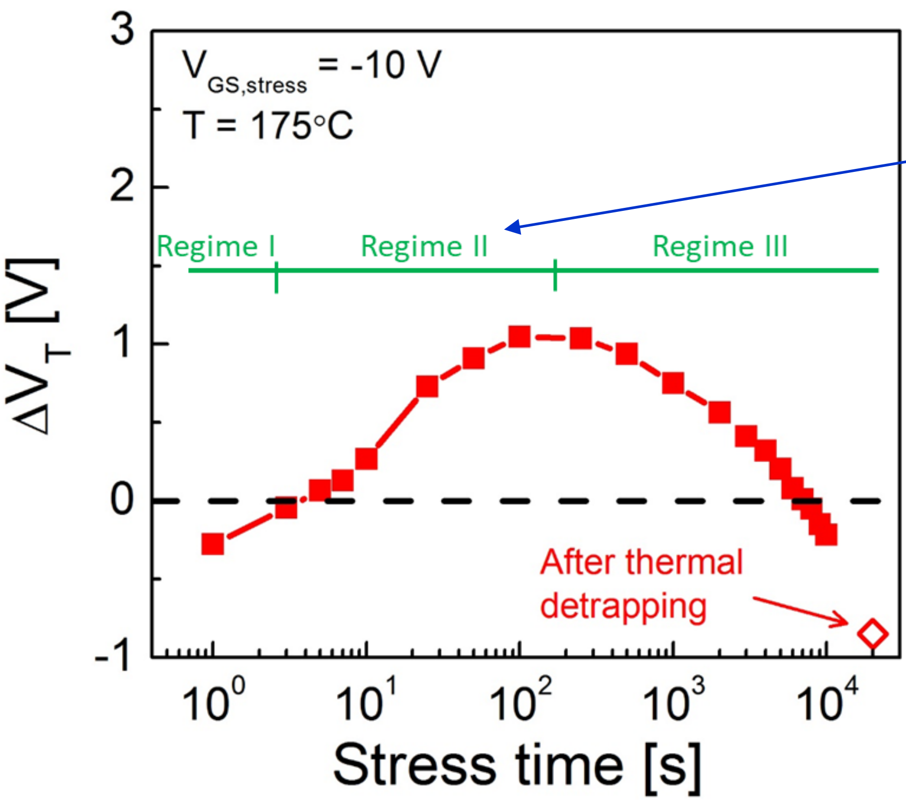
- Three regimes: Negative ΔV_T → positive ΔV_T → negative ΔV_T
- Permanent negative ΔV_T after final thermal detrapping

NBTI under harsher stress

High-voltage and high-temperature stress:

Trapping in GaN channel under gate edge (recoverable)





Guo, IRPS 2016

- Three regimes: Negative ΔV_T → positive ΔV_T → negative ΔV_T
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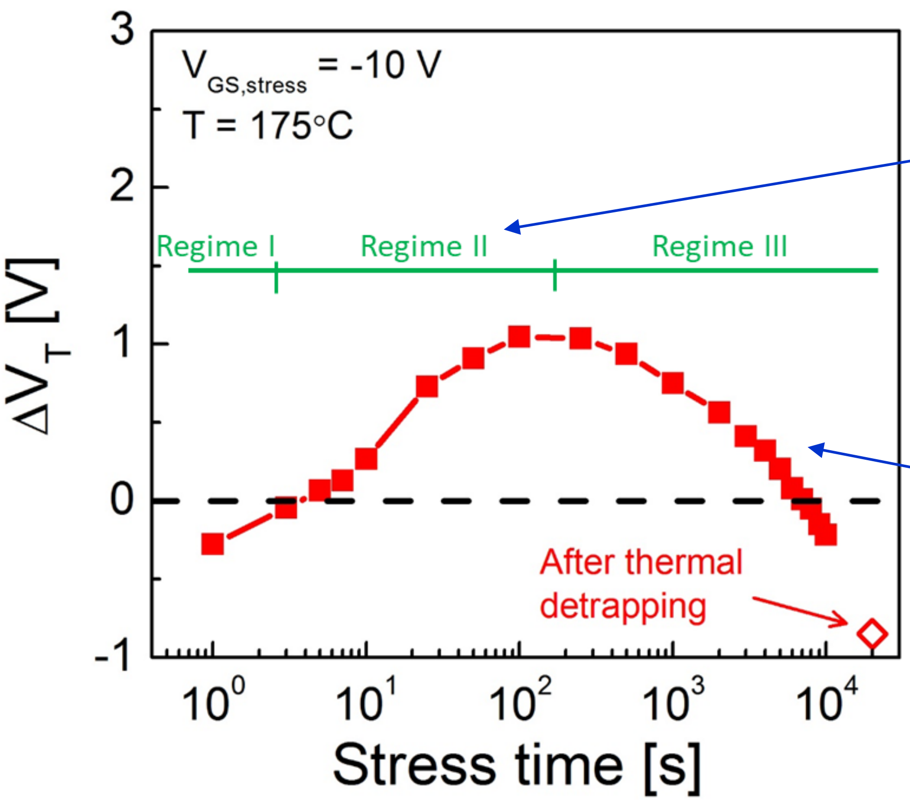
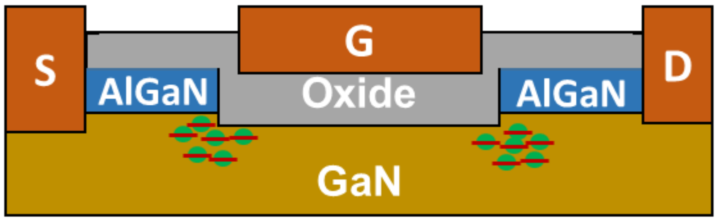
NBTI under harsher stress

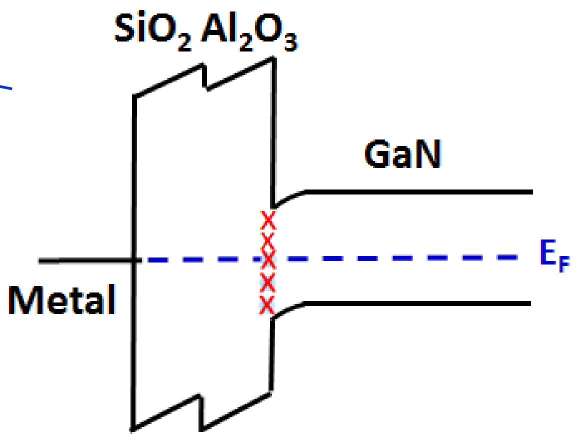
High-voltage and high-temperature stress:



Trapping in GaN channel under gate edge (recoverable)



Interface trap formation (permanent)



Guo, IRPS 2016

- Three regimes: Negative ΔV_T → positive ΔV_T → negative ΔV_T
- Permanent negative ΔV_T after final thermal detrapping

Conclusions

- PBTI and NBTI (benign stress):
  - recoverable ΔV_T, Δg_m due to electron trapping/detrapping in pre-existing oxide traps
  - Experimental observations well described by oxide trapping model

- Many avenues for mitigation → study Si high-k/MOS literature

- New degradation physics under harsher stress (NBTI):
  - recoverable $\Delta V_T > 0$, ΔS due to electron trapping in substrate
  - non-recoverable $\Delta V_T < 0$, Δg_m, ΔS due to interface state formation